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In the problems that follow, each cell in a battery provides a potential difference of 1.5 V. 2. In each of the circuits below, all the bulbs are identical. Write what you would expect the voltage drop across each bulb to be. A B C ©Modeling Workshop Project 2005 1 E3-Circuits - ws 3 v3.2

This book constitutes the refereed proceedings of the 13th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2003, held in Torino, Italy in September 2003. The 43 revised full papers and 18 revised poster papers presented together with three keynote contributions were carefully reviewed and selected from 85 submissions. The papers are organized in topical sections on gate-level modeling and characterization, interconnect modeling and optimization, asynchronous techniques, RTL power modeling and memory optimization, high-level modeling, power-efficient

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technologies and designs, communication modeling and design, and low-power issues in processors and multimedia.

Welcome to the proceedings of PATMOS 2005, the 15th in a series of international workshops. PATMOS 2005 was organized by IMEC with technical co-sponsorship from the IEEE Circuits and Systems Society. Over the years, PATMOS has evolved into an important European event, where researchers from both industry and academia discuss and investigate the emerging challenges in future and contemporary applications, design methodologies, and tools required for the development of upcoming generations of integrated circuits and systems. The technical program of PATMOS 2005 contained state-of-the-art technical contributions, three invited talks, a special session on hearing-aid design, and an embedded tutorial. The technical program focused on timing, performance and power consumption, as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and optimization in the nanometer era. The Technical Program Committee, with the assistance of additional expert reviewers, selected the 74 papers to be presented at PATMOS. The papers were divided into 11 technical sessions and 3 poster sessions. As is always the case with the PATMOS workshops, the review process was anonymous, full papers were required, and several reviews were carried out per paper. Beyond the presentations of the papers, the PATMOS technical program was enriched by a series of speeches offered by world class experts, on important emerging research issues of industrial relevance. Prof. Jan Rabaey, Berkeley, USA, gave a talk on "Traveling the Wild Frontier of Ultra Low-Power Design", Dr. Sung Bae Park, Seoul, gave a presentation on "DVL (Deep Low Voltage): Circuits and Devices", Prof.

The International Workshop on Power and Timing Modeling, Optimization, and Simulation PATMOS 2002, was the 12th in a series of international workshops previously held in several places in Europe. PATMOS has over the years evolved into a well-established and outstanding series of open European events on power and timing aspects of integrated circuit design. The increased interest, especially in low-power design, has added further momentum to the interest in this workshop. Despite its growth, the workshop can still be considered as a very focused conference, featuring high-level scientific presentations together with open discussions in a free and easy environment. This year, the workshop has been opened to both regular papers and poster presentations. The increasing number of worldwide high-quality submissions is a measure of the global interest of the international scientific community in the topics covered by PATMOS. The objective of this workshop is to provide a forum to discuss and investigate the emerging problems in the design methodologies and CAD-tools for the new generation of IC technologies. A major emphasis of the technical program is on speed and low-power aspects with particular regard to

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modeling, characterization, design, and architectures. The technical program of PATMOS 2002 included nine sessions dedicated to most important and current topics on power and timing modeling, optimization, and simulation. The three invited talks try to give a global overview of the issues in low-power and/or high-performance circuit design.

This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2006. The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts. Topical sections include high-level design, power estimation and modeling memory and register files, low-power digital circuits, busses and interconnects, low-power techniques, applications and SoC design, modeling, and more.

This book constitutes the thoroughly refereed post-conference proceedings of 19th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2009, featuring Integrated Circuit and System Design, held in Delft, The Netherlands during September 9-11, 2009. The 26 revised full papers and 10 revised poster papers presented were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on variability & statistical timing, circuit level techniques, power management, low power circuits & technology, system level techniques, power & timing optimization techniques, self-timed circuits, low power circuit analysis & optimization, and low power design studies.

This book constitutes the refereed proceedings of the 22nd International Conference on Integrated Circuit and System Design, PATMOS 2012, held in Newcastle, UK Spain, in September 2012. The 25 revised full papers presented were carefully reviewed and selected from numerous submissions. The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems, including reconfigurable hardware such as FPGAs. The technical program focus on timing, performance and power consumption as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and optimization.

th Welcome to the proceedings of PATMOS 2007, the 17 in a series of international workshops. PATMOS 2007 was organized by Chalmers University of Technology with IEEE Sweden Chapter of the Solid-State Circuit Society technical - sponsorship and IEEE CEDA sponsorship. Over the years, PATMOS has evolved into an important European event, where - searchers from both industry and academia discuss and investigate the emerging ch- lenges in future and contemporary applications, design methodologies, and tools - quired for the development of the upcoming generations of integrated circuits and systems. The

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technical program of PATMOS 2007 consisted of state-of-the-art technical contributions, three invited talks and an industrial session on design challenges in real-life projects. The technical program focused on timing, performance and power consumption, as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and optimization in the nanometer era. The Technical Program Committee, with the assistance of additional expert reviewers, selected the 55 papers presented at PATMOS. The papers were organized into 9 technical sessions and 3 poster sessions. As is always the case with the PATMOS workshops, full papers were required, and several reviews were received per manuscript.

This book constitutes the refereed proceedings of the 21st International Conference on Integrated Circuit and System Design, PATMOS 2011, held in Madrid, Spain, in September 2011. The 34 revised full papers presented were carefully reviewed and selected from numerous submissions. The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems and focus especially on timing, performance and power consumption as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis and optimization.

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